REMARKS

In the Office Action, the Examiner noted that claims 1-16 are pending in the application and that claims 1-4, 6-12 and 14-16 stand rejected. The Examiner further noted that claims 5 and 13 are objected to but would be allowable if written in independent form including all of the limitations of the base claims and any intervening claims. By this response claim 11 has been amended to correct for informalities pointed out by the Examiner and not in response to prior art. All other claims continue unamended by this response.

In view of the amendment above and the following discussion, the Applicant respectfully submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Thus, the Applicant believes that all of these claims are now in allowable form.

Objections

A. Claim 11

The Examiner has objected to claim 11 noting that in line 3, the term "rectors" should be "vectors".

In response, the Applicant has amended claim 11, as suggested by the Examiner, to recite "vectors" instead of "rectors".

Having made this change, the Applicant respectfully submits that the basis for the Examiner's objection to claim 11 has been removed. As such, the Applicant respectfully requests that the Examiner's objection to claim 11 be withdrawn.

B. Drawings

The Examiner objected to the drawings noting that in Figure 4, the equations for blocks 434 and 440 are identical. The Examiner noted that the components of the equation block 440 should be added according to page 6, lines 12-14 of the Applicant's Specification.

In response, the Applicant is herewith submitting a replacement sheet including Figure 4, corrected as suggested by the Examiner, such that the components of the equation block 440 are added according to page 6, lines 12-14 of the Applicant's Specification.

Having made this change, the Applicant respectfully submits that the basis for the Examiner's objection to the Applicant's figures, and specifically Figure 4, has been removed. As such, the Applicant respectfully requests that the Examiner's objection to the Applicant's figures be withdrawn.

C. Allowable Subject Matter

The Examiner has objected to claims 5 and 13 as being dependent upon a rejected base claim. The Examiner concludes that these claims would be allowable subject matter if rewritten in independent form including all the limitations of the base claim and any intervening claims.

The Applicant thanks the Examiner for indicating the allowable subject matter with respect to these claims. However, in view of the arguments set forth herein, the Applicant believes that claims 1 -16 as submitted herein are allowable over the prior art cited by the Examiner. Therefore, the Applicant respectfully requests that the foregoing objections to claims 5 and 13 be withdrawn.

Rejections

A. 35 U.S.C. § 102

The Examiner has rejected claims 1, 6, 7, 9-10, and 14-16 under 35 U.S.C. § 102(a) as being anticipated by the instant applications disclosed prior art (specifically figure 1). The rejection is respectfully traversed.

The Examiner alleges that regarding claim 1, the instant application's disclosed prior art shows all of the aspects of the Applicant's present invention including a pair of filters that teach the vector arithmetic structures (VAS) of the Applicant's invention. The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrik Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

The Applicant respectfully submits that Figure 1 of the instant application absolutely fails to teach, suggest or disclose each and every element of the claimed invention, arranged as in the claims of the Applicant. Specifically, the Applicant submits that Figure 1 of the instant application fails to teach, suggest or disclose each and every element of at least the Applicant' claim 1, which specifically recites:

> "An encoder, comprising:
> a constellation generator, responsive to an input bitstream to produce an impulse comprising an in-phase component and a quadrature component, said impulse defining symbols within a constellation of symbols;
> a pair of vector arithmetic structures (VAS), each VAS adapting a respective one of said in-phase and quadrature components to produce respective shaped in-phase and quadrature components; and
> a combiner, for combining said shaped in-phase and quadrature components to produce an encoded bitstream." (emphasis added).

The Applicant's invention of at least claim 1 is directed, at least in part, to an encoder including a pair of vector arithmetic structures (VAS) for adapting a respective one of in-phase and quadrature components to produce respective shaped in-phase and quadrature components. In support of at least claim 1 and specifically distinguishing the VAS of the Applicant's invention over the filters of Figure 1 of the instant application, the Applicant in the Specification specifically recites:

> "The constellation mapper 130 of FIG. 2 generates two orthogonal signals; namely, an in-phase signal I and a quadrature signal Q. The in-phase I and quadrature Q signals are coupled to, respectively, an in-phase vector arithmetic structure (VAS) 240 and a quadrature VAS 250. The operation of the in-phase VAS 240 and quadrature VAS 250 will be described in more detail below with respect to Figure. 3. Briefly, the

> vector arithmetic structures 240 and 250 perform various pulse shaping and other processing functions to produce respective output signals for further processing by combiner 160 to form a modulated signal. Unlike the in-phase filter 140 and quadrature filter 150 of the system 100 of FIG. 1, the in-phase VAS 240 and quadrature VAS 250 of the system 200 of FIG. 2 do not use multiplication operations. Rather, the vector arithmetic structures 240 and 250 utilize addition and shift operations, thereby achieving a high level of computational efficiency. The vector arithmetic structure is architected in a manner adapted to the pulse shaping function to which it is applied." (See Specification, page 4, line 20 through page 5, line 1).

It is very clear from at least the portion of the Applicant's Specification recited above that at least the VAS of the invention of the Applicant as recited in at least claim 1, distinguish the VAS of the Applicant's invention over Figure 1 of the instant application. More specifically, the Applicant presents and identifies at least one aspect of the VAS of the Applicant's invention that makes the Applicant's invention, at least with respect to claim 1, inventive over Figure 1 of the instant application. That is, the VAS of the Applicant's invention advantageously perform various pulse shaping and other processing functions utilizing addition and shift operations to produce respective output signals instead of using multiplication operations as in the filters of the encoder of Figure 1 of the instant application, thereby achieving a high level of computational efficiency.

The Applicant respectfully reminds the Examiner that inventors may act as their own lexicographers and use the specification to attribute specific meanings to terms in a patent claim. Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc., 262 Fed.3d 1258 1268(Fed. Cir. 2001). As such, claims must be read in view of the patent specification. Id. The Applicant further submits that for claims construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995). As such, the Applicant respectfully submits that the vector arithmetic structures of at least the Applicant's claim 1 must be interpreted as structures

that perform various pulse shaping and other processing functions utilizing addition and shift operations to produce respective output signals as defined in the Applicant's Specification. As such, the invention of the Applicant, at least with respect to independent claim 1, is clearly patentable over the prior art encoder of Figure 1 of the instant application.

In further support of at least claim 1, the Applicant in the Specification recites:

> "The VAS 300 of Figure 3 comprises a plurality of vector registers VR, a vector arithmetic unit (VAU), a vector shifter (VS), a vector accumulator (VA), a selector register (SR), an input data register (DR_{in}) and an output data register (DR_{out}). A first VAS 300 is used to implement the in-phase VAS 240 of the front end 200 of FIG. 2. A second VAS 300 is used to implement the quadrature VAS 250 of the system 200 of FIG. 2. It is noted that the in-phase VAS 240 and quadrature VAS 250 replace, respectively, the in-phase filter 140 and quadrature filter 150 of the system 100 of FIG. 1." (See Specification, page 5, lines 12-19).

The Applicant further recites:

> "Each data word (i.e., an upsampled and encoded constellation symbol) to be processed by the VAS 300 is received from the constellation mapper 130 and stored in the input data register DR_{in}. It is noted that upsampling each encoded constellation symbol may occur within the constellation mapper, as a separate function between the constellation mapper and VAS, or as an input stage of the VAS. It is also noted that non-upsampled data may be utilized within the context of VAS. Preferably, the Most Significant Bit (MSB) of the data word stored within the input register DR_{in} is coupled to the vector arithmetic unit VAU, which utilizes the MSB to determine whether an addition or subtraction operation is appropriate. The VAU operates as an adder if the MSB is in a first state, illustratively zero, or as a subtractor if the MSB is in a subtract (MSB) in a second state, illustratively one. Thus, the VAU selectively performs an addition operation or a subtraction operation using first and second input data words to produce an output data word.
>
> The arithmetic result produced by the VAU is stored in the vector shifter VS and the vector accumulator VA. The vector shifter VS is capable of storing N data words, denoted as R_0 through R_{N-1}. It is noted that each of the vector registers VR is capable of storing N data words, denoted as R_0 through R_{N-1}. Moreover, the vector accumulator VA is capable of storing N words denoted as AR_0 through AR_{N-1}. The vector

> shifter performs a left shift operation to provide the R_0 word to the output register DR_{OUT} for further processing by the combiner 160.
>
> The remaining (i.e., non-MSB) bits of each data word within the input register DR_{in} are stored in the selector register SR. The data stored within the selector register SR is used to index corresponding pre-computed values stored within the vector registers VR_1 through $VR_{M/2}$. Specifically, each non-MSB bit within the selector register SR has associated with it a corresponding vector register VR. Thus, depending upon the contents of the selector register SR, those vector registers VR associated with a non-MSB bit of a first state (e.g., a 1) provide their pre-computed values to a first input of the VAU. A second input of the VAU receives a previously accumulated vector from the vector accumulator VA. The VAU processes the previously accumulated vector and newly selected vector to produce a vector output which is stored in the vector shift register VS. The vector shift register provides the newly created vector to the vector accumulator VA and to the output register DR_{out}. The output register DR_{out} provides an output word to the combiner 160 for further processing." (See Specification, page 6, line 3 through page 7, line 6).

As evident from at least the portions of the Applicant's Specification presented above, the VAS of the Applicant's invention each comprise a plurality of vector registers VR, a vector arithmetic unit (VAU), a vector shifter (VS), a vector accumulator (VA), a selector register (SR), an input data register (DR_{in}) and an output data register (DR_{out}). There is absolutely no teaching, suggestion or disclosure in Figure 1 of the instant application for a VAS as taught in the Applicant's Specification as recited above and as claimed in at least the Applicant's claim 1.

Even further, the Applicant's Specification, at least as presented above, teaches that the VAS of the Applicant's invention utilizes addition and shift operations to produce respective output signals to be further processed by a combiner of the Applicant's invention. More specifically, the Applicant teaches that the Most Significant Bit (MSB) of a data word stored within the input register DR_{in} is coupled to the vector arithmetic unit VAU, which utilizes the MSB to determine whether an addition or subtraction operation is appropriate. Furthermore, an arithmetic result produced by the VAU is stored in the vector

shifter VS and the vector accumulator VA. The vector shifter performs a left shift operation to provide the R_0 word to the output register DR_{OUT} for further processing by the combiner. The Applicant further teaches that the remaining (i.e., non-MSB) bits of each data word within the input register DR_{in} are stored in the selector register SR. The data stored within the selector register SR is used to index corresponding pre-computed values stored within the vector registers VR_1 through $VR_{M/2}$. Specifically, each non-MSB bit within the selector register SR has associated with it a corresponding vector register VR. Thus, depending upon the contents of the selector register SR, those vector registers VR associated with a non-MSB bit of a first state (e.g., a 1) provide their pre-computed values to a first input of the VAU. A second input of the VAU receives a previously accumulated vector from the vector accumulator VA. The VAU processes the previously accumulated vector and newly selected vector to produce a vector output which is stored in the vector shift register VS. The vector shift register provides the newly created vector to the vector accumulator VA and to the output register DR_{out}. The output register DR_{out} provides an output word to the combiner 160 for further processing.

For at least the reasons stated above, the Applicant respectfully submits that there is absolutely no teaching, suggestion or disclosure in Figure 1 of the instant application for an encoder including at least a vector arithmetic structure (VAS) as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1, and more specifically for an encoder that includes at least a VAS that performs various pulse shaping and other processing functions utilizing addition and shift operations to produce a respective output signal. That is, the Applicant respectfully submits that Figure 1 of the instant application absolutely fails to teach, suggest or disclose each and every element of at least the VAS of the Applicant's claim 1 as required for anticipation, and as such does not anticipate at least the Applicant's claim 1.

Therefore, the Applicant submits that independent claim 1 is not anticipated by the teachings of Figure 1 of the instant application and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 10 recites similar relevant features as recited in claim 1. As such, the Applicant submits that independent claim 10 is also not anticipated by the teachings of Figure 1 of the instant application and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 6, 7, 9 and 14-16 depend either directly or indirectly from independent claims 1 and 10 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that dependent claims 6, 7, 9 and 14-16 are also not anticipated by the teachings of Figure 1 of the instant application. Therefore the Applicant submits that dependent claims 2-3, 8-10, 12-16, 18-20, and 22-23 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

B. 35 U.S.C. § 103(a)

The Examiner rejected claims 2-4, 8, 11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Figure 1 of the instant application in view of Corleto et al. (U.S. Patent 5,668,749, herein "Corleto"). The rejection is respectfully traversed.

Claims 2-4 and 8 are dependent claims that depend either directly or indirectly from the Applicant's claim 1. Claims 11 and 12 are dependent claims that depend directly and indirectly, respectively, from the Applicant's claim 10. The Examiner applied Figure 1 of the instant application for his rejection of claims 2-4, 8, 11 and 12 as described above for the Examiner's rejection of the Applicant's claims 1 and 10. The Examiner correctly concedes, however, that regarding claims 2 and 11-12, Figure 1 of the instant application does not disclose that the VAS comprises a plurality of vector registers and a vector

arithmetic unit. As such, the Examiner cites Corleto for teaching a plurality of registers for storing precomputed values from memories and selected vectors from the in-phase and quadrature registers. The Examiner further alleges that it would have been obvious to incorporate the teachings of Corleto into Figure 1 of the instant application. The Applicant respectfully disagrees.

As described above with regard to the Examiner's rejection of claim 1 and claim 10, Figure 1 of the instant application does not teach suggest, or make obvious the Applicant's invention with regard to claim 1 or claim 10 at least because Figure 1 fails to teach, suggest or describe an encoder including at least a VAS that advantageously performs various pulse shaping and other processing functions utilizing addition and shift operations to produce respective output signals. As such, and at least for the reasons set forth above indicating that Figure 1 of the instant application does not teach suggest, or make obvious the Applicant's invention with regard to claim 1 and claim 10, the Applicant respectfully submits that dependent claims 2-4, 8, 11 and 12, which depend either directly or indirectly from independent claims 1 and 10, are also not rendered obvious by Figure 1 of the instant application.

Even further, the Applicant submits that the teachings of Corleto alone also do not teach the invention of the Applicant at least with regard to claims 1, 2-4, 8, 10-11 and 12. That is, Corleto teaches a circuit for performing arithmetic operations in a demodulator. In Corleto, a circuit for determining a radius value and a phase value from an in-phase signal and a quadrature signal iteratively approximates the phase value and the radius value based upon initial in-phase signal and quadrature signal preferably using the coordinate rotational digital computer (CORDIC) algorithm. The circuit of Corleto includes a multi-task arithmetic unit, memory, and a controller. The multi-task arithmetic unit includes registers, multiplexers, shift registers, and an adder to perform various arithmetic operations. The circuit further includes dynamic memory for storing the solutions at different points in time of the radius value and phase value, which are

subsequently used in the filtering of radius values and phase values. (See Corleto, Abstract).

However, in contrast to the invention of the Applicant, at least with respect to claims 1, 2-4, 8, 10-11 and 12, there is absolutely no teaching, suggestion or disclosure in Corleto for an encoder including at least a vector arithmetic structure (VAS) component utilized to produce a shaped component by utilizing addition and shift operations as taught in the Applicant's Specification and claimed by at least the Applicant' claims 1 and 10. As such, and at least because Corleto does not teach, suggest or make obvious the Applicant's claims 1 and 10, the Applicant further submits that Corleto also does not teach, suggest or make obvious the Applicant's claims 2-4, 8, 11 and 12, which depend either directly or indirectly from the Applicant's claims 1 and 10, respectively.

Furthermore, the Applicant submits that there is no suggestion or motivation to combine the teachings of Figure 1 of the instant application and the teachings of Coleto.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Applicant submits that there is absolutely no motivation or suggestion in the encoder of Figure 1 of the instant application for the combination of the references. That is, there is nothing in the description of Figure 1 of the instant application that indicates a desire or need for an arithmetic circuit such as the circuit of Corleto. In addition, the Applicant submits that there is also absolutely no motivation or suggestion in Corleto for the combination of the references. More specifically, the teachings of Corleto for a circuit for performing arithmetic operations in a demodulator do not suggest or motivate the combination of the circuit of Corleto with the encoder of Figure 1 of the instant application. That is, there is absolutely no teaching, suggestion or motivation in Corleto for combining the arithmetic circuit of Coleto with an encoder such as the encoder of Figure 1 of the instant application in an attempt to teach the invention of the Applicant. Neither Corleto nor Figure 1 of the instant application teach or suggest how the arithmetic circuit of Corleto would be capable of operating in the encoder of Figure 1 of the instant application, remembering that hindsight is strictly forbidden.

Moreover, the Applicant submits that even if there was a motivation or suggestion to combine the references (which the Applicant believes that there is none), the teachings of Figure 1 of the instant application and Corleto, either alone or in any allowable combination, fail to teach the invention of the Applicant at least with respect to claim 1 and claim 10. That is, the Applicant submits that the teachings of Corleto fail to bridge the substantial gap between the Applicant's invention at least with respect to claims 1 and 10, and the teachings of Figure 1 of the instant application. More specifically, and as discussed above, Figure 1 of the instant application fails to teach, suggest or make obvious at least a vector arithmetic structure (VAS) that advantageously performs various pulse shaping and other processing functions utilizing addition and shift operations to produce respective output signals to be further processed by a combiner. Even further, if Figure 1 of the instant application were combined with the teachings of Corleto,

the combination also fails to teach, suggest or make obvious the Applicant's claims 1 and 10 at least with respect to a vector arithmetic structure (VAS) to produce respective shaped in-phase and quadrature components and other processing functions utilizing addition and shift operations to produce respective output signals as taught in the Applicant's Specification and claimed by at least the Applicant's claims 1 and 10.

As such and at least because the teachings of Figure 1 of the instant application and Corleto, alone or in any allowable combination, fail to teach, suggest or make obvious the Applicant's claims 1 and 10 for at least the reasons described above, the Applicant further submits that the teachings of Figure 1 of the instant application and Corleto, alone or in any allowable combination, also fail to teach, suggest or make obvious the Applicant's invention with respect to dependent claims 2-4, 8, 11 and 12, which depend either directly or indirectly from the Applicant's claims 1 and 10, respectively and recite further limitations thereof.

Therefore, the Applicant respectfully submits that claims 2-4, 8, 11 and 12, as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

Conclusion

Thus the Applicant submits that none of the claims, presently in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicant believes that all of these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 383-1396 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E/Wall

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Dated: 12/7/04

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Amendments to the Drawings

The attached drawing sheet includes changes to Figure 4. This sheet, which includes Figure 4, replaces the original sheet including Figure 4.

In Figure 4, the components of the equation block 440 are added according to page 6, lines 12-14 of the Applicant's Specification as suggested out by the Examiner.

Attachment: Replacement Sheet